4Links®

SpaceWire @400Mbps

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Why oversampling

- SpaceWire only transitions one signal per clock cycle (Grey coded)
- Sampling rate can be close to data rate (1.5x)
- Data extraction with oversampling is simpler
- Visit 4Links.co.uk article: SpaceWire-on-FPGA

Over Sampling verses Clock Recovery

Over Sampling Approach

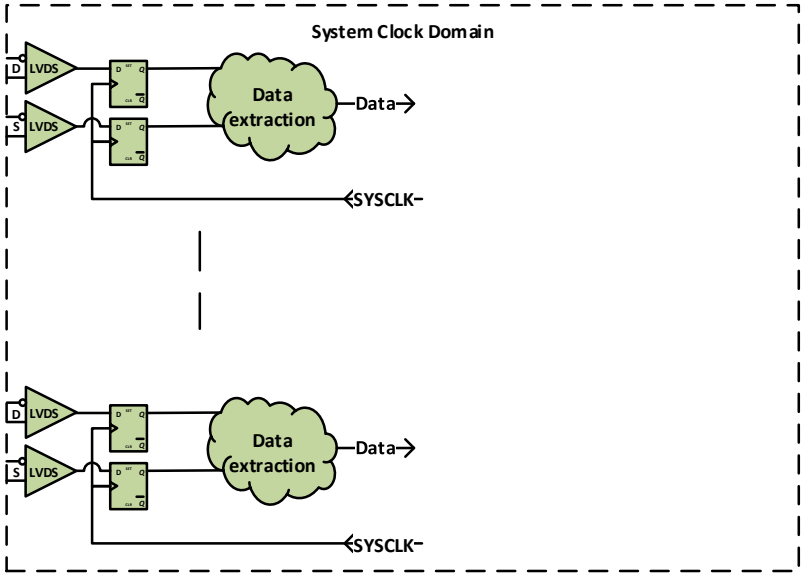
- Pro's
  - Easy to achieve 400Mbps
  - Synthesis tool Friendly
  - Fully synchronous design
  - Single clock domain
  - Simple timing constraints
- Con's
  - Higher Power consumption
  - Metastability at sampling FF

Clock Recovery Approach

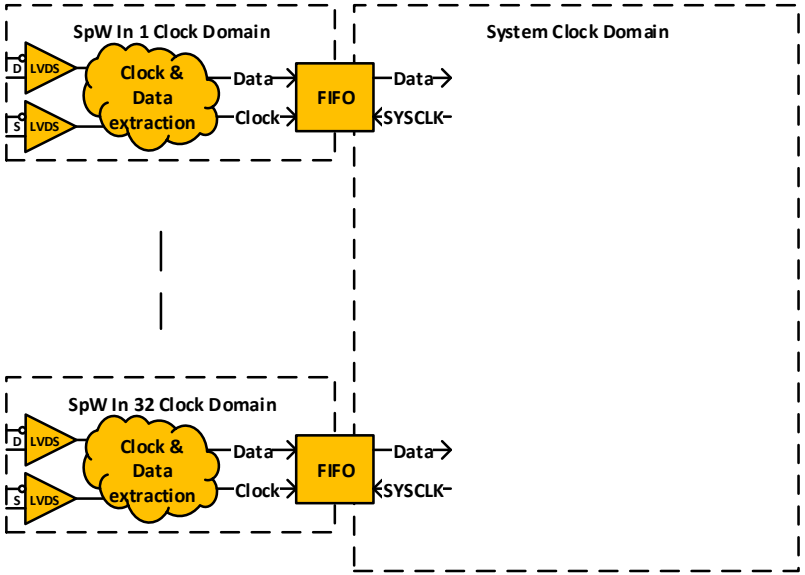
- Pro's
  - Lower power consumption
- Con's
  - Difficult to achieve 400Mbps
  - Synthesis tool unfriendly
  - Asynchronous design
  - Multiple clock domains
  - Complex timing constraints
  - Metastability at FIFOs

Clock Domains

1-32 SpaceWire ports
1 Clock Domain

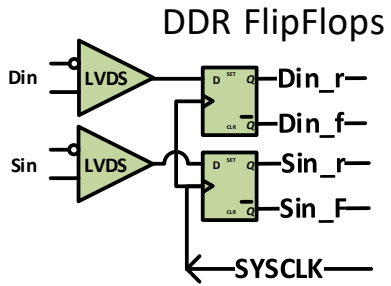


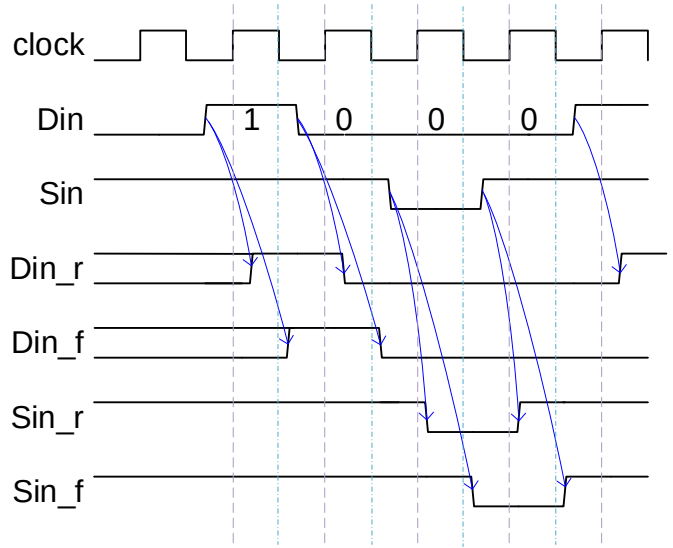
1-32 SpaceWire ports
2-33 Clock Domains



Example Front End

```
-- Use LVDS input buffers
u_din_buffer: IBUFDS generic map (DIFF_TERM => TRUE, IOSTANDARD => "LVDS")
port map( I => Din_p, IB=> Din_n, O => din );
u_sin_buffer: IBUFDS generic map (DIFF_TERM => TRUE, IOSTANDARD => "LVDS")
port map( I => Sin_p, IB=> Sin_n, O => sin );
```






```
-- Register inputs, sampling at DDR
u_din_iddr: iDDR generic map ( DDR_CLK_EDGE => "OPPOSITE_EDGE", INIT_Q1 => '0', INIT_Q2 => '0', SRTYPE => "ASYNC")
port map( D => din, Q1 => din_r, Q2 => din_f, C => clock, CE => '1', S => '0', R => '0' );
u_sin_iddr: iDDR generic map ( DDR_CLK_EDGE => "OPPOSITE_EDGE", INIT_Q1 => '0', INIT_Q2 => '0', SRTYPE => "ASYNC")
port map( D => sin, Q1 => sin_r, Q2 => sin_f, C => clock, CE => '1', S => '0', R => '0' );
```

~~A~~SYNC

- 4Links has dropped Patents on oversampling
  - Keeping 400Mbps achievable in FPGA
- 4Links has opensource IP
  - BSD License for easy adoption
  - Visit: www.4links.co.uk for details
  - Email: info@4Links.co.uk to download the IP

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