SpaceWire IP
IP4L-XXXX-X

Overview

4Links' SpaceWire IP is based on a simplified version of the CoDec (Coder/Decoder) used in its test equipment for SpaceWire. Thousands of SpaceWire ports of this test equipment have proved to be interoperable with all the SpaceWire designs to which they have been connected. The IP is also flight proven as the fundamental interconnect on a satellite. It also complements the test solutions and cabling on offer by 4Links.

The IP is supplied as a complete package:

- Standard, easy to use FIFO-style interface to user logic (Data Flow Channel, DFC)
- HDL simulation test bench
  - Traffic generator
  - Traffic logger (logging all the received traffic)

The simulation test bench enables you to easily see how the IP operates and how to integrate it into your design. A traffic generator (dfc9_master) and logger (dfc9_slave) are included in the test-bench connecting to the 4Links standard Data Flow Channels (used to connect to all 4Links IP). The generator and logger use a simple text based file allowing easy modification and checking of the vectors, so you can customise it to model the actual data in the design.

The IP is implemented in VHDL, but is designed to be instantiated in Verilog modules with minimal effort.

IP Solutions

The IP solutions available from 4Links are listed in the table. IP is always in development so for an up to date list of IP and features please contact 4Links.

FPGA technologies supported by 4Links IP are

- Xilinx®
  - Spartan®-6
  - Virtex®-7, Kintex®-7
  - Kintex®UltraScale®
- MicroSemi
  - ProASIC®3
  - RTAX®, RTG®4

Other technologies are being added continuously, please contact 4Links for more details.

<table>
<thead>
<tr>
<th>IP</th>
<th>Performance</th>
<th>LUTs</th>
<th>BRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>CoDec</td>
<td>&gt;200MHz</td>
<td>423</td>
<td>1</td>
</tr>
<tr>
<td>RMAP Target</td>
<td>&gt;150MHz</td>
<td>503</td>
<td>0</td>
</tr>
<tr>
<td>Routing Switch 4port</td>
<td>&gt;150MHz</td>
<td>5528</td>
<td>5</td>
</tr>
<tr>
<td>FDIR</td>
<td>Contact 4Links</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Based on Spartan®6 -3 device

The performance is the FPGA internal clock
Data Flow Channel

All IP implements the inter-module communications using the Data Flow Channels. Two data flow channels in a bi-directional connection is called a Data Flow Link.

The Data Flow Channel implements a simple handshake driven interface with an Output Ready (OR) and an Input Ready (IR) signal pair. The OR signal always follows the data flow direction and the IR signal is always against the data flow direction.

Either the Source or Sink can hold off a transaction by keeping the respective OR or IR signals low. A data transfer is completed when both IR and OR are high on a rising clock edge. The Source will always drive OR low after a transfer, meaning that all transfers will be two cycles in length. This simple interface enables easy clock domain crossing (FIFO type) implementations by the user.

Key Features

**CoDec**
- No clock domain crossings
- Fully synchronous design
- Oversampling (4Links Patent)
- Only a single clock timing constraint required

**RMAP Target**
- 16MByte address range

**Routing Switch**
- 2 to 32 ports

**General**
- Test-benches with Out-of-Box and Integration tests